

EXHIBIT B



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/007,869	01/09/2006	6766501	SYNP 107	8180

36454 7590 02/28/2006

SYNOPSIS, INC. C/O HAYNES BEFFEL & WOLFELD LLP
P.O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER

ART UNIT

PAPER NUMBER

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HAYNES BEFFEL & WOLFELD LLP

DOCKETED: 3/7/06 BY: gk
ACTION: US - Patent Owner's Statement
DUE DATES: 4/28/06 - Final
DOCKET NO: SYNP 107-0

HAYNES BEFFEL & WOLFELD LLP
MAR 06 2006
RECEIVED

Order Granting / Denying Request For Ex Parte Reexamination	Control No. 90/007,869	Patent Under Reexamination 6766501	
	Examiner St. John Courtenay III	Art Unit 3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed 09 January 2006 has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a) ☐ PTO-892, b) ☒ PTO-1449, c) ☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

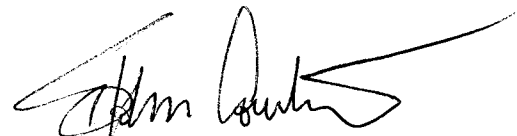
For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

- a) ☐ by Treasury check or,
b) ☐ by credit to Deposit Account No. _____, or
c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).



St. John Courtenay III
Primary Examiner
Art Unit: 3992

Application/Control Number: 90/007,869
Art Unit: 3992

Page 2

Response to Request for *ex parte* Reexamination

1. Reexamination has been requested for claims 1 and 8 of U.S. Patent number 6,766,501 ('501 patent).
2. A substantial new question of patentability affecting at least claim 1 of United States Patent number 6,766,501 is raised by the request for *ex parte* reexamination.
3. The '501 patent is currently assigned to:
SYNOPTSYS, INC.
700 EAST MIDDLEFIELD ROAD
MOUNTAIN VIEW, CALIFORNIA 94043
4. The '501 patent application filing date was Aug. 12, 2002 and the patent issued on July 20, 2004.
5. The '501 patent application is a continuation of application 09/275,502, filed on March 24, 1999, now U.S. Pat. No. 6,434,733.
6. In the request for reexamination, the Patent Owner states that the following references raise a substantial new question of patentability with respect to claims 1 and 8 for which reexamination is requested:
 - Barbagallo et al., "Scan Insertion Criteria for Low Design Impact", Proc IEEE VLSI Test Symposium, 1996 (hereinafter Barbagallo-1").

Application/Control Number: 90/007,869
Art Unit: 3992

Page 3

- Barbagallo et al., "Layout-driven scan chain partitioning and reordering", IEEE European Test Workshop, 1996 (hereinafter "Barbagallo-2").

7. The aforementioned newly cited references were not of record in the file of the '501 patent and are not cumulative to the art of record in the original file.

8. It is agreed that there exists a substantial likelihood that at least the Barbagallo-1 reference would have been considered important by a reasonable Examiner in deciding whether or not at least claim 1 was patentable, for the reasons discussed *infra*:

9. As per independent claim 1, Barbagallo-1 teaches a computer implemented process for electronic design automation, said process comprising the steps of:

- receiving a scannable netlist of an integrated circuit, said scannable netlist comprising a scan chain [Barbagallo-1 generates a scannable netlist based on a netlist. Barbagallo-1 describe scan insertion tools that partition cells in an integrated circuit netlist into scan chains, see e.g., page 1, col. 2, lines 38 to page 2, col. 1, line 37; see also admission of Patent Owner (page 5 of the request for reexamination received Jan 9, 2006)];

Application/Control Number: 90/007,869
Art Unit: 3992

Page 4

- partitioning said scan chain into a plurality of sets of re-orderable scan cells, wherein partitioning information which describes the scan cells of each set is generated [e.g., Barbagallo-1 teaches driving the partitioning process with logical constraints only, see page 2, col. 2, under the heading "3. Proposed Approach": i.e., "In our first implementation, we chose to drive the **partitioning** process with *logical constraints* only ..."] ; and
- based on said partitioning information, re-ordering scan cells of said scan chain during layout processes of said integrated circuit design, said step of re-ordering only re-ordering scan cells of a same set [e.g., Barbagallo-1 teaches that physical data are used to select the ordering inside each scan chain, page 2, col. 2, under the heading "3. Proposed Approach": i.e., "In our first implementation, we chose to drive the **partitioning process** with *logical constraints* only, while *physical data* are used to select the **ordering** inside each scan chain. In Fig. 1, a pseudo-code of the algorithm is presented."].

Application/Control Number: 90/007,869
Art Unit: 3992

Page 5

Conclusion

10. All claims are subject to reexamination.

11. Extensions of time under 37 C.F.R §1.136(a) will not be permitted in this proceeding because the provisions of 37 C.F.R. §1.136 apply only to "an Applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. §305 requires that *ex parte* reexamination proceedings "will be conducted with **special dispatch**" (37 C.F.R. §1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 C.F.R. §1.550(c).

12. The Patent Owner is reminded of the continuing responsibility under 37 C.F.R. § 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent number 6,766,501 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

Application/Control Number: 90/007,869
Art Unit: 3992

Page 6

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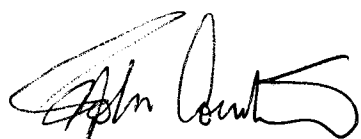
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Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed: St. John Courtenay III
(Monday - Friday 9:00 AM - 5:30 PM)

Primary Examiner
Central Reexamination Unit 3992
(571) 272-3761

Conductees:
MR. R. A. SPRE-CRU-3992
Eric K. Smith


ST. JOHN COURTENAY III
PRIMARY EXAMINER

PTO/SB/08B (08-03)

Approved for use through 07/31/2006. OMB 0651-0031
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known		
		Patent Number	6,766,501 90/007, 869	
		Issue Date	July 20, 2004	
		First Named Inventor	Duggirala et al.	
		Art Unit	3992	
		Examiner Name	COURTENAY	
Sheet 1	of 1	Attorney Docket Number		SYNP 107

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SC	C1	S. Barbagallo et al. "Scan Insertion Criteria for Low Design Impact", Proc IEEE VLSI Test Symposium, 1996, consisting of 7 pages.	
SC	C2	S. Barbagallo et al "Layout-driven Scan Chain Partitioning and Reordering" , IEEE European Test Workshop, 1996, consisting of 3 pages.	

Examiner Signature	S. COURTENAY	Date Considered	2-27-2006
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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		Art Unit	3992
		Examiner Name	COURTENAY
Sheet 1	of 1	Attorney Docket Number	SYNP 107

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SC	C1	S. Barbagallo et al. "Scan Insertion Criteria for Low Design Impact", Proc IEEE VLSI Test Symposium, 1996, consisting of 7 pages.	
SC	C2	S. Barbagallo et al "Layout-driven Scan Chain Partitioning and Reordering", IEEE European Test Workshop, 1996, consisting of 3 pages.	
SC	C3	Lin et al. "Layout-driven Chaining of Scan Flip-Flops", IEEE Proc. Comput. Digit. Tech., Vol. 143, No. 6, November 1996, pp. 421-425	
SC	C4	Chen et al. "Layout Driven Selecting and Chaining of Partial Scan Flip-Flops", 33rd Design Automation Conference June 1996, consisting of 6 pages.	
SC	C5	Hirech et al. "A New Approach to Scan Chain Reordering Using Physical Design Information", IEEE Proceedings of the Proceedings International Test Conference, 1998 pp. 348-355.	
SC	C6	Kobayashi et al. "A VLSI Scan-Chain Optimization Algorithm for Multiple Scan-Paths", IEICE Trans. Fundamentals, Vol. E82-A, No. 11 November 1999, pp. 2499-2504.	
SC	C7	K.D. Boese et al. "Scan Chain Optimization: Heuristic and Optimal Solutions", Internal Report, UCLA CS Dept., October 1994, pp.1-19. Available at http://citeseer.csail.mit.edu .	
SC	C8	Cirasella et al. "The Asymmetric Traveling Salesman Problem: Algorithms, Instance Generators, and Tests", ALENEX 2001 Proceedings, Springer Lecture Notes in Computer Science 2153, pp. 32-59.	
SC	C9	Berthelot et al. "An Efficient Linear Time Algorithm For Scan Chain Optimization and Repartitioning", ITC International Test Conference, IEEE 2002, pp. 781-787.	
SC	C10	S. Barbagallo et al. "Scan Chain Partitioning and Re-ordering Based on Layout Information: An Industrial Experience", DATE98: Design, Automation and Test in Europe, February 1998, 5 pages.	

Examiner Signature	S. COURTENAY	Date Considered	2-27-2006
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